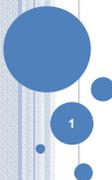


MATH CO-PROCESSOR 8087

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INTRODUCTION



- 8087 was the first math coprocessor for 16-bit processors designed by Intel.
- It was built to pair with 8086 and 8088.
- The purpose of 8087 was to speed up the computations involving floating point calculations.
- Addition, subtraction, multiplication and division of simple numbers is not the coprocessor's job.
- It does all the calculations involving floating point numbers like scientific calculations and algebraic functions.

INTRODUCTION



- By having a coprocessor, which performs all the calculations, it can free up a lot of CPU's time.
- This would allow the CPU to focus all of its resources on the other functions it has to perform.
- This increases the overall speed and performance of the entire system.
- This coprocessor introduced about 60 new instructions available to the programmer.
- All the mnemonics begin with "F" to differentiate them from the standard 8086 instructions.
- For e.g.: in contrast to ADD/MUL, 8087 provide FADD/FMUL.

INTRODUCTION

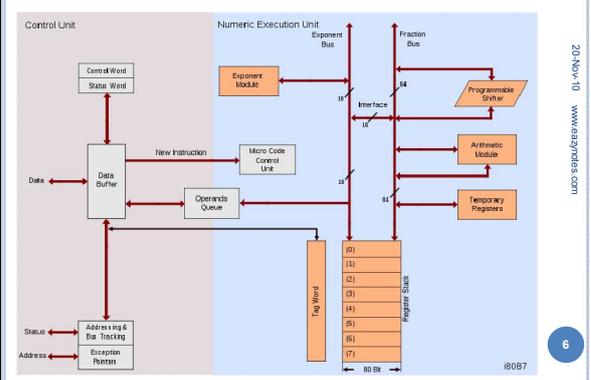


- Math coprocessor is also called as:
 - Numeric Processor Extension (NPX)
 - Numeric Data Processor (NDP)
 - Floating Point Unit (FPU)

ARCHITECTURE OF 8087

- 8087 coprocessor is designed to operate with 8086 microprocessor.
- The microprocessor and coprocessor can execute their respective instructions simultaneously.
- Microprocessor interprets and executes the normal instruction set and the coprocessor interprets and executes only the coprocessor instructions.
- All the coprocessor instructions are ESC instructions, i.e. they start with "F".

ARCHITECTURE OF 8087



The diagram illustrates the internal architecture of the 8087 coprocessor. It is divided into three main sections: the Control Unit, the Numeric Execution Unit, and the Fraction Bus. The Control Unit contains a Central Word Status Word, a Data Buffer, a Micro Code Control Unit, and an Operands Queue. The Numeric Execution Unit includes an Exponent Module, a Fraction Bus, a Programmable Shifter, an Arithmetic Module, and Temporary Registers. The Fraction Bus is connected to the Exponent Module via a 16-bit Exponent Bus and to the Programmable Shifter via a 16-bit Interface. The Arithmetic Module is connected to the Fraction Bus via a 61-bit bus. The Temporary Registers are connected to the Fraction Bus via an 80-bit bus. The Control Unit also includes a Status Register with Addressing & Bus Tracking and Exception Pointer, and a Tag Word. The entire coprocessor is labeled as 8087.

ARCHITECTURE OF 8087

- The internal structure of 8087 coprocessor is divided into two major sections:
 - Control Unit (CU)
 - Numerical Execution Unit (NEU)

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CONTROL UNIT (CU)

- It interfaces coprocessor to the microprocessor system bus.
- It also synchronizes the operation of the coprocessor and the microprocessor.
- This unit has a Control Word, Status Word and Data Buffer.
- If an instruction is ESC instruction, then coprocessor executes it.
- If not, then microprocessor executes.

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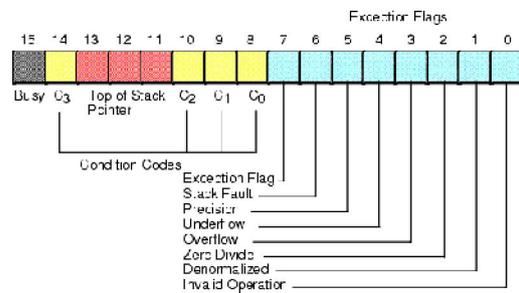
NUMERIC EXECUTION UNIT (NEU)

- This unit is responsible for executing all coprocessor instructions.
- It has an 8 register stack that holds the operands for instructions and result of instructions.
- The stack contains 8 registers that are 80-bits wide.
- Numeric data is transferred inside the coprocessor in two parts:
 - 64-bit mantissa bus
 - 16-bit exponent bus

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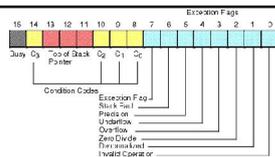
STATUS REGISTER



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STATUS REGISTER

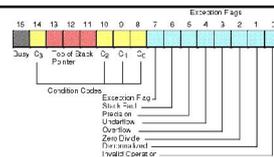


- Status Register tells the overall status of 8087 coprocessor.
- It is a 16-bit register.
- It is accessed by executing the FSTSW instruction.
- This instruction stores the contents of status register into memory.
- Once the status is stored in memory, the bit positions of the status register can be examined.

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STATUS REGISTER



- **Busy:** It indicates that the coprocessor is busy executing the task.
- **Condition Codes (C₀-C₃):** They indicate various conditions about the coprocessor.
- **Top of Stack:** It indicates a register as top of stack register, out of the eight stack registers.
- **Exception Flag:** It is set if any of the exception flag bits (SF, PR, UF, OF, ZD, DN, IO) are set.

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STATUS REGISTER

- Stack Fault: It is not available in 80387 and above. It is active only in 80387 and above.
- Precision: It indicates that the result has exceeded the selected precision.
- Underflow: It tells if the result is too small to fit in a register.
- Overflow: It tells if the result is too large to fit in a register.

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STATUS REGISTER

- Zero Divide: It indicates that you try to divide a non-zero value by zero.
- Denormalized: It indicates that at least one of the operand is de-normalized.
- Invalid Operation: It indicates an invalid operation. For e.g.: pushing more than eight items onto the stack, attempting to pop an item off an empty stack or taking the square root of a negative number.

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CONTROL REGISTER

- Control Register controls the operating modes of 8087.
- It is also a 16-bit register.
- It performs rounding control and precision control.
- It is also used to do masking and unmasking of the exception bits that correspond to the rightmost six bits of the status register.
- FLDCW instruction is used to load the value into control register.

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CONTROL REGISTER

- Rounding Control: It determines the type of rounding or truncating to be done.
- Precision Control: It sets the precision of the result.
- Exception Masks: It determines that whether an error effects the exception bits in the status register.
 - If it is one, then the corresponding error is ignored.
 - If it is zero and the corresponding error occurs, then it generates an interrupt, and the corresponding bit in status register is set.

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TAG REGISTER

TAG 7	TAG 6	TAG 5	TAG 4	TAG 3	TAG 2	TAG 1	TAG 0
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Tag Values:
 00 = Valid
 01 = Zero
 10 = Invalid
 11 = Empty

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TAG REGISTER

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- Tag Register is used to indicate the contents of each register in the stack.
- There are total 8 tags (Tag 0 to Tag 7) in this register and each tag uses 2 bits to represent a value.
- Therefore, it is a 16-bit register.

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PIN DIAGRAM OF 8087

GND 1 AD ₁₄ 2 AD ₁₃ 3 AD ₁₂ 4 AD ₁₁ 5 AD ₁₀ 6 AD ₉ 7 AD ₈ 8 AD ₇ 9 AD ₆ 10 AD ₅ 11 AD ₄ 12 AD ₃ 13 AD ₂ 14 AD ₁ 15 AD ₀ 16 NC 17 NC 18 CLK 19 GND 20	8 0 8 7	40 V _{CC} 39 AD ₁₅ 38 A ₁₆ /S ₁ 37 A ₁₇ /S ₂ 36 A ₁₈ /S ₃ 35 A ₁₉ /S ₄ 34 B _{HE} /S ₇ 33 RQ/GT ₁ 32 \overline{INT} 31 RQ/GT ₀ 30 NC 29 NC 28 $\overline{S_2}$ 27 $\overline{S_1}$ 26 $\overline{S_0}$ 25 OS ₀ 24 OS ₁ 23 BUSY 22 READY 21 RESET
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INTERFACING OF 8086 AND 8087

- Multiplexed address-data bus lines are connected directly from 8086 to 8087.
- The status lines and the queue status lines are connected directly from 8086 to 8087.
- The Request/Grant (RQ/GT₀ and RQ/GT₁) signals of 8087 are connected to RQ/GT₀ and RQ/GT₁ of 8086.
- BUSY signal of 8087 is connected to TEST pin of 8086.

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Thank You

Have a Nice Day

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